In the claims:

Please substitute the following full listing of claims for the original claim listing.

1. (Original) A semiconductor integrated circuit having array transistors in memory cells and logic transistors wherein said array transistors have a spacing of the minimum feature size, F, said memory cells having an area of $12F^2$ or less and said logic transistors having an effective channel length of 0.7F or less, an effective gate dielectric thickness of twenty Angstroms or less, a dual work function semiconductor gate with maximum depletion thickness of 1.5 Angstroms of equivalent oxide thickness in the inversion mode and a source drain contact resistance of 3×10^{-8} or less.

2. (Original) A semiconductor integrated circuit including

array transistors having metal gate conductors encapsulated by a diffusion barrier including a thick cap insulator and a borderless source/drain contact at a spacer adjacent said thick cap insulator, and

logic transistors having silicided contacts, extension implants and a dual work function semiconductor gate having an impurity concentration of greater than 4×10^{20}.

3. (Original) A semiconductor integrated circuit as recited in claim 2, wherein said array transistors are separated by a minimum lithographic feature size.

4-15 (Cancelled)